

# OpenATE QSPI

## 3U PXI QUAD Digital PE and I2C IO Card

- 4 site x 8 input / output channels, IO dynamically configurable
- 64 M of on-board vector memory per channel
- -1 ~ +10 VOH VOL VIH VIL per channel
- 32 PMU per board
- 10 MHz data rate
- 4 I2C Master on 400KHz CLK
- 4 SPI Master on 10MHz CLK
- 4 32 bit/ 10 ns counter
- Operates as a stand-alone card or with up to 7 additional synchronous slave boards
- API & Pattern Editor



## Description

The QSPI represents a multi-function of performance and capabilities for PXI-based digital instrumentation. The QSPI offers high performance pin electronics and 4 I2C masters and 4 32bit counter in a compact, 3U PXI form factor. Each card can function as a quad sites I2C/SPI device tester, multiple cards can be interconnected, supporting up to 64 sites. The QSPI also supports deep pattern memory by offering 64 M of on-board vector memory with dynamic per pin direction control and with test rates up to 10 MHz.

## Features

The QSPI supports -1 ~ +10 VOH VOL VIH VIL per channel and 32 PMU per board. The QSPI offers 1 timing sets, 2 driver TG Edges, 2 strobe TG Edges and four drive data formats are supported.

RTZ (Return To Zero), RTO (Return To One), NRZ (Non Return To Zero), SBC (Surround By Complement) which can providing flexibility to create a variety of bus cycles and waveforms to test board and box level products.

## On-Board Memory

The QSPI offers 64 M of vector memory per channel. Programmable pattern cycle times up to  $2^{32}$  or infinite. There are pattern symbols including 0, 1, L, H, X, Z, J, Q.

## Compatibility

All OpenATE Interfaces PXI cards comply with the PXI Specification 2.0 (issued Aug. 2000)

## Software

The QSPI is supplied with API and Pattern Editor. Pattern Editor is a software tool that edits test patterns.

## Application

- Automatic Test Equipment(ATE)
- Consumer Digital Functional Test
- Digital Pattern Generation
- I2C salve Device Testing

**OpenATE Inc.**

*The Open Solution for IC Tester*

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# OpenATE QSPI

## Specifications

<b>• Pin Electronics</b>		<b>• Logic Sequencer</b>	
I/O Channels	32, per board resource	Micro-Instructions	REPEAT; FC
Test rate	10MHz	Pattern Symbols	0, 1, L, H, X, Z, J, Q
Input Level (Vih/ Vil)	-1 ~ +10V per channel	LMSYNC to PXI Trigger Bus	For Sync With other Instruments
Output Level (Voh/Vol)	-1 ~ +10V per channel	Ignore Fail By LM Address	YES
<b>• Timing</b>		Vector Memory	64M(length) × 32(channels)
Period Resolution	10nS	Programmable pattern cycle times	2 <sup>32</sup> or infinite
Pin TG Edge Resolution	10nS	<b>• I2C/SPI/COUNTER</b>	
Minimum Pulse Width	10nS	I2C master	4/ 400KHz
Timing Sets	1	SPI master	4 /10MHz
Driver TG Edges	2, per pin resource	32 bits counter	4/ 10nS resolution
Strobe TG Edges	2, per pin resource	<b>• Physical Properties</b>	
		Bus Interface	PXI
<b>• Formatter (Change On The Fly)</b>		Dimensions	3U
Format Sets	1	Power Requirements	3.3V@3A, 5V@3A 12V@0.5A
RTZ, Return To Zero RTO, Return To One NRZ, Non Return To Zero SBC, Surround By Complement		System Clock	100MHz
<b>• PMU</b>		Bus & Signals	8 PXI Trigger bus lines for parallel test
Number of PMU	32	<b>• Environmental</b>	
PMU Accuracy	1.00%	Operating Temperature	0 ~ 50°C
Number of IRange x 8	I1: ±2uA/I2: ±8uA I3: ±32uA/I4: ±128uA I5: ±512uA/I6: ±2mA I7: ±8mA/I8: ±32mA	Storage Temperature	-20 ~ 70°C
Number of VRange x 1	E1: -1V ~ +3V	<b>• Software</b>	API & Pattern Editor
<b>• PXI Compliance</b>		<b>• Maximum boards in one system</b>	16
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